REMARKS/ARGUMENTS

Claims 1-6, 8-15, and 17-28 are pending in the present application. Claims 7 and 16 have been canceled. Claims 1, 11, 17, and 21 have been amended. No new matter has been added to the amended claims. Reconsideration of the claims is respectfully requested.

Obviousness Rejections of Claims 1-6 and 8-28

The office action rejection claims 1-6 and 8-28 as being obvious in light of U.S. Patent 4,719,369 to Asano et al. and U.S. Patent 5,721,548 to Choe et al.

The Applicants have amended the claims to address these rejections. For example, claim 1 has been amended to recite:

"a digital encoder circuit coupled to receive the 2^N output signals of the comparators, the digital encoder circuit encoding the 2^N output signals of the comparators into N digital signals that represent an N-bit binary value, the binary value indicating how many of the 2^N output signals of the comparators are HIGH." See e.g., the present application at page 9, lines 3-24.

The function of subtractor circuit 31 is described in Asano et al. at col. 4, lines 8-17:

> Assume that an output "11010" is produced by the A/D converter circuit 30 when a P channel MOS transistor 20 with maximum drain current is obtained, and an output "01011" thereof when the same transistor 20 with minimum drain current is obtained. If the input A of the subtractor circuit 31 is set to "11010", an output "00000" is obtained when the input B, that is the output of the A/D converter circuit 30, is "11010", and an output of "01111" when the input B is "01011".

In Asano et al., the substractor 31 receives a 5-bit signal from A/D circuit 30 (at its B input) and subtracts this 5-bit signal from the 5-bit signal at its A input to generate a 5-bit output signal. The least significant four bits of the 5-bit output signal of substractor 31 are used to control transistors 2-5. See Asano et al. col. 4, lines 17-24.

On the other hand, the digital encoder circuit of the present invention converts the 2^N digital output signals of the A/D converter into N digital output signals that indicate how

many of the comparator output signals are HIGH. The digital encoder circuit substantially reduces the number of digital output signals of the A/D converter.

This feature is advantageous because the A/D converter of the present invention can include significantly more comparators (2^N) than there are transistors (N) in the impedance matching circuit. Having more comparators allows the A/D converter to generate an output signal that indicates the voltage at the first transistor with more precision. The output signals of the A/D converter can have significantly more bits than there are transistors in the impedance matching circuit. The digital encoder circuit converts the 2^N output signals of the A/D converter into N digital signals that are used to turn the transistors in the impedance matching circuit ON or OFF.

For at least these reasons, it is respectfully submitted that amended claim 1 and its dependent claims are novel and nonobvious over the cited prior art references.

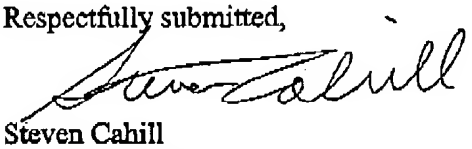
In light of the amendments, claim 1 is novel and nonobvious over the cited prior art references for similar reasons. The other pending claims are also allowable for similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Steven Cahill
Reg. No. 44,578

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400 Fax: 415-576-0300

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